San José State University
Department of Aviation &Technology
Tech 63 Digital Circuits, Fall 2017

Course and Contact Information

Instructor: Dr. Pouya Ostovari

Office Location: IS 106

Telephone: (408)-924-3917

Email: pouya.ostovari@sjsu.edu

Office Hours: MW: 14:30 – 15:30

Class Days/Time: M: 18:00 – 19:45 Lecture
W: 18:00 – 20:45 Lab

Classroom: Lectures: IS 216
Lab: IS 117

Prerequisites:
Tech 30

Course Format

The course relies on lecture and lab materials presented in class and students are strongly encouraged to attend.

Course Description

Logic gates emphasizing TTL and CMOS. Design techniques. Combinational circuits, counters, registers, multiplexers, de-multiplexers, encoders, decoders, and logic gates. Course may include familiarization with digital programming of FPGAs

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

1. Understand the principles of single logic gate devices and serial manipulation of logic streams.

2. Comprehend the working knowledge of flip-flops and related devices.

3. Describe counters and registers.

4. Understand interfacing with the analog world.

5. Explain the operations of encoders, decoders, multiplexers and De-multiplexers.

Required Texts/Readings

Textbook

Floyd, Thomas L., Digital Fundamentals. 11th Edition. Upper Saddle River, New Jersey: Prentice Hall, 2014

Lab Manual

Buchla and Joksch Experiments in Digital Fundamentals, eleventh edition lab manual

Upper Saddle River, New Jersey: Prentice Hall, 2003

Course Requirements and Assignments

You will answer selected questions for each chapter. Homework and lab assignments will be posted on Canvas. You should submit your work via Canvas by the due date.

Final Examination

The final exam will be comprehensive, covering all material presented in class.

Grading Information

Homework	10%
Quizzes	15%
Midterm 1	10%
Midterm 2	10%
Lab	30%
Final Exam	25%

The final grade will be determined according to the following scale:

A+ 96-100	B+ 87-89	C+ 77-79	D+ 67-69	F <60
A 93-95	B 83-86	C 73-76	D 63-69	
A- 90-92	B- 80-82	C- 79-72	D- 60-62	

1. Check continuously your standing in the class on Canvas (https://sjsu.instructure.com). Notify the instructor immediately if there is an error in any of your grades.

2. All late assignments submitted up to 7 calendar days after the due date and time will have a penalty of 10% per day.

3. **Assignments submitted after 7 calendar days of the due date will not be accepted and they will be recorded as 00.**

4. There will not be any makeup quiz, but your lowest quiz grade will not be considered.

Classroom Protocol

Class participation and attendance are strongly encouraged. Use of cell-phones are not allowed. Laptop computers and tablet are allowed only for taking lecture notes and related work to the lectures.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

Students with Special Need

If you need special accommodation, please contact Accessible Education Center at your earliest convenience. You can find more information at http://www.sjsu.edu/aec/faculty/index.html.

Tech 165 Wireless Communications Technologies, Fall 2017 Course Schedule/Outline

Tentative Calendar*

Week	Topics, Readings, Assignments, Deadlines
1, Aug 28th	• Introduction, Course Organization, Orientation • Chapter 1
2, September 4th	• Chapter 1 continued
3, September 19th	• Chapter 2
4, September 26th	• Chapter 2 continued
5, October 2th	• Chapter 3
6, October 9th	• Chapter 3 continued • Review for exam
7, October 16th	• Midterm exam 1
8, October 23th	• Chapter 4
9, October 30th	• Chapter 4 continued
10, November 6th	• Chapter 5 • Review for exam
11, November 13th	• Chapter 5 • Review for exam
12, November 20th	• Midterm exam 2
13, November 27th	• Chapter 6
14, December 4th	• Chapter 7
15, November 11th	• Review for final
Monday, December 18	• Final exam, 17:15-19:30

* Subject to change with fair notice

Holidays:
Monday, September 4 Labor Day - Campus Close
Friday, November 10 Veteran's Day - campus closed
Wednesday, November 22 Non-instructional holiday (no classes held)
Thursday - Friday, November 23 - 24 Thanksgiving Holiday - campus closed

You can find the calendar at http://info.sjsu.edu/static/policies/calendar-fall.html

Tentative List of Experiments*
Lab#1 Lab Instrument Familiarization
Lab#2 Constructing a Logic Probe
Lab#3 Number Systems
Lab#4 Logic Gates
Lab#5 More Logic Gates

Lab#6 Interpreting Manufacturing Data Sheets
Lab#7 Boolean Theorems and De Morgan's Theorems
Lab#8 Logic Circuit Simplification
Lab#9 Perfect Pencil Machine
Lab#10 Experiment 11 Adder and Magnitude Comparator
Lab#11 Experiment 12 Combinational Logic Using Multip0lexers
Lab#12 Experiment 13 Combinational Logic Using Demultiplexers
Lab#13 Experiment 14 The D Latch and D Flip Flop

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