

San José State University
Computer Science Department
CS 147, Section 02
Computer Architecture Spring, 2020

Instructor(s):	Dr. Chung-Wen (Albert) Tsao
Office Location:	Duncan Hall Room 282
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Email:	chung-wen.tsao@sjsu.edu (Once the class starts, use Canvas Inbox)
Office Hours:	W/M 09:15– 10:15 am
Class Days/Time:	MW 10:30 - 11:45 am
Classroom:	Boccardo Business Center 004
Prerequisites:	CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)
Class Meeting Dates:	Jan 23, 2020 - May 11, 2020

Class Format

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on [Canvas](http://sjsu.instructure.com) at <http://sjsu.instructure.com>. You are responsible for regularly checking the most updated messages and uploaded materials there.

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.

- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.

Required Textbooks

Computer Organization and Design – The Hardware/Software Interface, 5th Edition

Authors: David A. Patterson, John L. Hennessy

Isbn: 9780124077263

Publication Date: 10/10/2013

Publisher: Elsevier

Other Readings

Computer Architecture, 5th Edition

Author: John L. Hennessy

ISBN: 9780123838728

Publication Date: 09/29/2011

Publisher: Elsevier

Logic & Computer Design Fundamentals, 5th Edition

Author: Mano & Kime

ISBN: 9780131989269

Publication Date: 06/15/2007

Publisher: PEARSON

Computer Organization and Architecture, 10th Edition

Author: Stallings

ISBN: 9780134101613

Publication Date: 01/12/2015

Publisher: Pearson

The C Programming Language, 2nd Edition

Author: Kernighan And Ritchie ("K&R"),

ISBN: 0131103628

Publication Date: 01/01/2012

Publisher: Prentice Hall

Other technology requirements / equipment / material

You will be **required** to bring a [wireless laptop](#) to all classes for pop quizzes.

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in [University Policy S12-3](http://www.sjsu.edu/senate/docs/S12-3.pdf) at <http://www.sjsu.edu/senate/docs/S12-3.pdf>.

Homework, Midterm and Final exam are expected for this class. Homework is due on Canvas by class starting time on the due date. Each assigned problem requires a solution and an explanation (or work) detailing how you arrived at your solution. Cite any outside sources used to solve a problem. When grading an assignment, I may ask for additional information.

NOTE that [University policy F69-24](http://www.sjsu.edu/senate/docs/F69-24.pdf) at <http://www.sjsu.edu/senate/docs/F69-24.pdf> states that "Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading."

Grading Information

- Pop quizzes 10%
- Homework 20%
- Project 1 10%
- Project 2 10%
- Midterm 1 15%
- Midterm 2 15%
- Final Exam 20%

Exam scores may be curved only if the average is below 65%

Final grades will not be adjusted in any way - so an 89.9% is still a B+.

No incomplete grades will be given.

The grading scale is as follows:

A+ beyond 92.5%	A 92.5%	A- 90.0%
B+ 87.5%	B 82.5%	B- 80.0%
C+ 77.5%	C 72.5%	C- 70.0%
D+ 67.5%	D 60.0%	F below 60.0%

Note that "All students have the right, within a reasonable time, to know their academic scores, to review their grade- dependent work, and to be provided with explanations for the determination of their course grades." See [University Policy F13-1](http://www.sjsu.edu/senate/docs/F13-1.pdf) at <http://www.sjsu.edu/senate/docs/F13-1.pdf> for more details.

Classroom Protocol and Other Notes

- **Absences in attending the first two lectures will be dropped out from the class.**
- **No late assignments will be accepted without advanced arrangement with the instructor.**
- **No incomplete grades will be given.**
- **No exam may be taken before or after the scheduled time for any reason.**
- **There is no make-up quiz, assignment, project, or midterm/final exam.**
- **No extra credit will be assigned. Grades will not be adjusted in any way.**
- Do not ask for special treatment. The rules for this course apply to everyone equally.

- Cheating will not be tolerable; a ZERO will be given to any cheated assignment/exams, and it will be reported to the Department and the University.
- Do NOT share/post online any course materials, PPT slides, or homework solutions.
- Audio or video recording of the lectures are NOT allowed.
- Use of electronic devices during exams is NOT allowed.
- You are required to check Canvas for reading/assignments.
- The information on this syllabus is subject to change; changes, if any, will be carefully explained in class, and it is your responsibility to become aware of them.

Once the class starts, use Canvas Inbox to email me for a faster response. I check the Canvas Inbox emails much more often than my school emails.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' [Syllabus Information web page](http://www.sjsu.edu/gup/syllabusinfo/) at <http://www.sjsu.edu/gup/syllabusinfo/>

Course Schedule (This schedule is subject to change. Any change will be communicated via Canvas with fair notice.)

Week	Date	Topics, Readings, Assignments, Deadlines
1	01/27, 29	Introduction
2	02/03,05	MIPS Instructions
3	02/10,12	MIPS Instructions
4	02/17,19	Arithmetic for Computers
5	02/24,26	Arithmetic for Computers
6	03/02	Midterm 1, Logic Design
7	03/09,11	Logic Design
8	03/16,18	The Processor
9	03/23,25	The Processor
10	03/30	Spring break
11	04/06	Midterm 2, Memory Hierarchy
12	04/13,15	Memory Hierarchy
13	04/20,22	Memory Hierarchy
14	04/27,29	Memory Hierarchy
15	05/04,06	Virtual Memory
16	05/11	Review
Final Exam	05/15	09:45-12:00am, Friday

[SJSU ACADEMIC YEAR CALENDAR 2019/20](#)