CHANG Y. CHOO[1]
Professor
Department of Electrical Engineering
San Jose State University
San Jose, California 95192-0084
(408)924-3980, Mobile: (408)766-1028
e-mail: chang.choo@sjsu.edu

PROFESSIONAL BIOGRAPHY:
Dr. Chang Choo is currently Professor of Electrical Engineering and Director of DSP/FPGA Laboratory at San Jose State University, San Jose, California. He was Senior Member of Technical Staff with Altera Corporation for two years from January 1999. From 1986 to 1998, he was a faculty member of Electrical Engineering Department at Worcester Polytechnic Institute, Worcester, Massachusetts, and, later, at San Jose State University. He taught and did research on DSP, video and image compression/processing, and computer architecture. He is currently doing research/consulting/teaching on FPGA-based DSP systems design, including video/audio compression, wireless communications and adaptive filtering. He has over 80 journal and conference publications and 7 patents in these areas. He was a member of Technical Committee with several professional conferences including SPIE, DesignCon, and DSP World/ICSPAT. He was a consultant for various companies including Philips Semiconductor, National Semiconductor (acquired by Texas Instruments), Ricoh Innovations and Skybox (acquired by Google). Dr. Choo received his PhD in computer and systems engineering from Rensselaer Polytechnic Institute, Troy, NY.

EDUCATION:
Ph.D. (1986), Computer & Systems Engineering, Rensselaer Polytechnic Institute., Troy, NY.
M.S. (1982), Operations Research and Statistics, Rensselaer Polytechnic Institute., Troy, NY.
M.S. (1981), B.S. (1977), Industrial Engineering, Seoul National University, Seoul, Korea.

PERSONAL:
Naturalized U.S. Citizen; Married with two children.

LANGUAGE SKILLS:
Fluent in Korean; Can read well, with limited speaking ability in Japanese.

SELECTED EXPERIENCE:
San Jose State University, Department of Electrical Engineering, August 1991-1998, 2001-present, Professor; Director of FPGA/DSP Laboratory. Director of Image Processing Laboratory. Conducting research on hardware and algorithm development for video compression and processing (including MPEG-2, MPEG-4, and H.264). Also doing research on FPGA DSP IP design, DSP architectures, and algorithms. Teaching courses on embedded system design and architecture, digital image processing, digital video compression, digital signal processing and architectures, and FPGA DSP system design.

CDI Mobile Technology, San Jose, CA, December 2006-January 2009, Consulting Technologist. Conducted marketing and development of location-based image/video processing software and hardware for mobile telephone applications.

RealChip Communications, Sunnyvale, CA, November 2000-March 2002, System Architect and Senior Manager. Conducted SOC design of VOIP and video-over-IP processors.

[1] March 2015

Altera Corporation, San Jose, CA, DSP IP Business Unit, January 1999-October 2000, Senior Member of Technical Staff. Conducted technical marketing on DSP, wireless communications, video/imaging and voice over IP. Also, conducted research and development of FPGA-based DSP IPs on various CDMA, FIR filters, and video/imaging circuits.

iQuest, San Jose, CA, August 1997-December 1998, CEO/CTO, Managed all aspects (business and technical) of the MPEG-2 nonlinear video editor software development project.

National Semiconductor, Santa Clara, CA, Corporate Technology Group, May 1994-February 1997, Resident Scholar (part-time), Consultant. Conducted research on very low bit-rate videoconferencing (H.320, H.324, and proprietary algorithms) system development using TI C54 and C80.

In addition, consulted a number of companies including **Philips Semiconductor, Lockheed Martin, FutureTel/Innovacom, Ateme, Datum, Ricoh Innovation, and Skybox** in the areas of video and audio compression/processing algorithms including MPEG-2, MPEG-4, H.264 multimedia DSP processor architectures, and Voice-over-IP DSP ASIC/FPGA design.

Worcester Polytechnic Institute, Department of Electrical Engineering, September 1986 - July 1991, Assistant Professor of Electrical Engineering. Conducted research on multiprocessor system development for image coding, 2D/3D object representation and recognition, and mobile robot navigation. Worked with other faculty to develop Image Processing Laboratory and Image Processing Seminar. Developed Digital Signal Processing Laboratory (TI DSPs) and served as Director. Taught digital logic design and microprocessor system design courses at undergraduate level, and computer architecture and computer vision courses at graduate level.

Korea Atomic Energy Research Institute, Seoul, Korea, Energy Systems Laboratory, August 1979-May 1981, Researcher. Developed a national energy system optimization model using linear/nonlinear programming and input/output analysis. Completed projects on long-term and short-term energy demand forecasting using regression and time series analysis.

CURRENT ACADEMIC SERVICE:
2012-Present, Member of University RTP Committee
2010-Present, Chair of EE Digital Curriculum Committee

SELECTED FUNDED PROJECTS:
[1] Volkswagen Electronics Research Laboratory (Belmont, California), Illumination- and View-Independent Object Recognition Algorithm for Driverless Car, February 2015-Deceember 2015, $50,000.
[2] ETRI (Korea), Study of FPGA Architecture for Echo Canceller Accelerator, July 2010-January 2011, $90,000.
[3] ETRI (Korea), Study of FPGA Architecture for Speech and Audio Convergence Media Accelerator, July 2009-January 2010, $80,000.
[4] ETRI (Korea), FPGA Design of Hardware Accelerator IPs for Super Wideband Audio Codec, September 2008-January 2009, $100,000.
[5] ETRI (Korea), Convergent and Bundled Services in U.S. Telecommunications Markets, 2007, $25,000.
[6] ETRI (Korea), MVNO and MVOIP: Regulatory Regimes in the United States, 2006, $23,000.
[7] ETRI (Korea), A study on LM Dialing Parity and MVNO in the United States, 2004, $25,000.

[8] Philips Semiconductor, COMPARATIVE PERFORMANCE EVALUATION OF PHILIPS TRIMEDIA PROCESSOR, June 1, 1997 - August 31, 1997, $30,000.
[9] FutureTel/Innovacom, MPEG-2 Encoder ASIC Design, May 1996 - September 1996, $25,000.
[10] National Semiconductor, C50-Based NSV (National Semiconductor Video) Compression System Development, December 1995 - June 1996, $15,000.
[11] National Semiconductor, Performance Evaluation of H.26P TMN4/SAAC (Very Low Bitrate Video Coding Standard for Public Switching Telephone Network), November 1994 - June 1995, $19,000.
[12] National Science Foundation, Developing Advanced Digital Design Laboratory Using Field Programmable Gate Array Development Systems, September 1992 - February 1995, $66,832 (50% non-NSF contribution).
[13] Texas Instruments, Digital Signal Processor Equipment Grant, January 1990, $100,000.

SELECTED COURSES TAUGHT:
FPGA Design of Video and Image Processing Algorithms (1-day short course given in 2010 and 2009 SPIE Electronic Imaging Conference), FPGA DSP Systems Design (4-day short course to engineers and managers, as well as semester-long graduate course); Advanced VLSI Design for DSP and Communications; Logic Circuit Design; Digital Design Using HDL; Digital Signal Processing; Advanced Computer Architectures; Programmable Architectures for DSP (TI DSP Processor Architectures); Digital Image Processing; Microprocessor Systems Design; Advanced Topics in Computer Vision, Graphics and CAD.

SELECTED PROFESSIONAL SERVICES:
[1] Associate Editor, Journal of Real-Time Image Processing, Springer, February 2013-January 2015.
[2] Member of Program Committee, Real-Time Image and Video Processing, IS&T/SPIE Electronic Imaging 2013.
[3] Member of Technical Committee, DesignCon, 2010, 2009.
[4] Member of ICSPAT-2000 Technical Review Committee, Dallas, Texas, Oct. 16-19, 2000.
[5] Session Chair (Applications of Artificial Neural Networks in Image Processing and VLSI Session) for IS\&T/SPIE Symposium on Electronic Imaging: Science and Technology, San Jose, California, 2006-1995.
[6] Publicity Chairman for 1997, 1996, 1995, 1994, 1993, and 1992 Annual Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, California.
[7] Workshop Co-organizer (Software Stuff) for Frontiers in Education Conference, San Jose, California, November 2-6, 1994.
[8] Session Chair (Session IV) for Fourth Annual TMS320 Educators Conference, Dallas, Texas, October 21-22, 1994 (sponsored by Texas Instruments).
[9] Member of Technical Program Committee for the 4th University of New Brunswick Artificial Intelligence Symposium, Fredericton, N.B., Canada, September 19-21, 1991.
[10] Director, Korean Information Technology Network (KIN), San Jose, CA.
[11] Reviewed technical papers for *ETRI Journal*, *IEEE Transactions on Image Processing*, *IEEE Transactions on Neural Networks*, *IEEE Transactions on Circuits and Systems for Video Technology*, *IEEE Transactions on Robotics and Automation*, *Journal of Robotic Systems*, and proposals for National Science Foundation.

SELECTED PATENTS:
[1] "Apparatus and method for implementing efficient arithmetic circuits in programmable logic devices," U.S. Patent Nos. 7,058,675 (2006) and 7,124,161 (2006) (with A. Hazanchuk).
[2] "Motion vector based frame insertion process for increasing the frame rate of moving images," U.S. Patent Nos. 5,943,096 (1999) and 6,621,864 (2003).

[3] "Hashing-Based Vector Quantization," U.S. Patent Nos. 5,832,131 (1998) and 5,991,455 (1999) (with X. Ran).
[4] "Syntax Based Arithmetic Coder and Decoder," U.S. Patent No. 5,587,710, 1997 (with X. Ran, et al.).

SELECTED EXPERT WITNESS ENGAGEMENT

Parties: SanDisk Corp. v. LSI Corp./Agere Systems, Inc.
Time Frame: Spring 2010
Primary Contact: Judge Hon. William Alsup
Contact's Firm: U.S. District Court, Northern District of California, San Francisco Division
Contribution: Rule 706 Expert (Expert appointed by Federal Court)
Relevant expertise: MP3 and MPEG-2 audio and video compression software and hardware

Parties: Civolution B.V. v. Doremi Labs, Inc.
Time Frame: Spring 2015
Primary Contact: Dr. Cliff Maier, Esq.
Contact's Firm: Mayer Brown LLP
Contribution: Expert Witness
Relevant expertise: FPGA hardware and HDL for digital watermarking for video server

SELECTED PUBLICATIONS

[1] "FPGA-Based Hardware Accelerator for Feature Extraction in Automatic Speech Recognition," Int. J. lnfo. Commun. Converg. Eng. 13(3): 145-151, Sep. 2015 (with Y.U. Chang and I.Y. Moon).
[2] "Novel Write request handling for Static Wear Leveling in Flash Memory (SSD) Controller," Int. J. lnfo. Commun. Converg. Eng. 11(3): 147-154, Sep. 2013 (with P. Gajipara and I.Y. Moon).
[3] "FPGA Design of a Real-Time Edge Enhancing Smoothing Filter," IS&T/SPIE Electronic Imaging, Burlingame, California, Feb. 3-7, 2013 (with N. Pandya).
[4] "An FPGA-Based Embedded Wideband Audio Codec System," 19th international Conference on Field Programmable Logic and Applications, Prague, Czech Republic, Aug. 31-Sep. 2, 2009.
[5] "Design of High-Performance Adaptive FIR Filters Using FPGA," DesignCon, Santa Clara, California, Feb. 4-7, 2008.
[6] "FPGA-Based Hardware Accelerator for Rank and Median Filters for Image processing," 4th Conference on New Exploratory Technologies, Seoul, Korea, Oct. 25-27, 2007 (with P. Verma).
[7] "FPGA-Based Embedded Acoustic Echo Canceller System," 4th Conference on New Exploratory Technologies, Seoul, Korea, Oct. 25-27, 2007 (with W. Zhang).
[8] "Economic Effects of Indirect Access Regime in the Mobile Telecommunication Market," 35th Research Conference on Communication, Information and Internet Policy, George Mason University School of Law, Arlington, Virginia, Sep. 28-30, 2007 (with B.W. Kim).
[9] "An Embedded Adaptive Filtering System on FPGA," GSPx Conference, Santa Clara, CA, Oct. 30-Nov. 2, 2006 (with P. Padmanabhan, et al.).
[10] "Implementation of Texas Instruments TMS32010 DSP Processor on Altera FPGA," GSPx Conference, Santa Clara, CA, September 27-30, 2004 (with J. Chung, et al.).
[11] "Mapping LMS Adaptive Filter IP Core to Multiplier-Array FPGA Architecture for High Channel-Density VOIP Line Echo Cancellation," IP Based SOC Design Workshop, Grenoble, France, October 30-31, 2002.
[12] "A Memory Reduction Scheme for Multi-Channel Echo Canceller Implementation," Proc.

III International Conf. Acoustics, Sound, and Signal Processing, Salt Lake City, Utah, pp.3301-3304, May 7-11, 2001 (with H. Elabd).
[13] "Designing High-Performance Echo Canceller for VOIP," *DSP Engineering Mag.*, vol.2, no.1, pp. 12-26, 2000.
[14] "Constrained Variable-Bit-Rate Control Algorithm for MPEG-2 Encoder," Proc. SPIE, vol. 3974, pp.133-143, Image and Video Communications and Processing 2000, B. Vasudev; T.R. Hsing; A.G. Tescher; R.L. Stevenson; Eds. (with D. Zhang).
[15] "Optimization of 2D median filtering algorithm for VLIW architecture," Proc. SPIE, vol.3970, pp. 70-79, Media Processors 2000, S. Panchanathan; V.M. Bove; S.I. Sudharsanan; Eds. (with M. Tang).
[16] "Design and Implementation of Digital FIR Filters Using Altera FIR Compiler," *DSP and Multimedia Magazine*, 1999.
[17] "Video Applications for Distributed Arithmetic," tutorial workshop paper, ICSPAT-99, Orlando, Florida, November 1999.
[18] "Syntax-Based Arithmetic Video Coding for Very Low Bitrate Visual Telephony," Proc. IEEE Intern. Conf. Image Processing, Washington, DC, pp.II410-II413, Oct. 22-25, 1995 (with X. Ran).
[19] "Evaluation of Design Parameters for a Cache Vector Quantization System," Proc. First IEEE Conference on Image Processing, Austin, Texas, pp. 129-133, Nov. 13-16, 1994 (with N. M. Nasrabadi).
[20] *H.26P/TMN2-NSC: National Semiconductor Implementation of ITU H.26P Draft Recommendation on Video Coding for Narrow Telecommunication Channels at < 64 kbits/s*, Confidential Technical Report, Corporate Technology Group, National Semiconductor, Santa Clara, California, September, 1994 (with X. Ran, et al.).
[21] "Dynamic Finite-State Vector Quantization of Digital Images," *IEEE Transactions on Communications*, vol.42, no.5, pp.2145-2154, May 1994 (with N. M. Nasrabadi and Y. Feng).
[22] "Performance Analysis of a Vector Quantizer with Cache Memory," Proc. 27th Annual Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, California, pp. 956-960, Nov. 1-3, 1993 (with B. A. Cicchetto and N. M. Nasrabadi).
[23] "Interframe Hierarchical Address-Vector Quantization," *IEEE Journal on Selected Areas in Communications*, vol. 10, no. 5, pp. 960-967, June 1992 (with N. M. Nasrabadi and J. U. Roy).
[24] "Hopfield Network for Stereo Vision Correspondence," *IEEE Transactions on Neural Networks*, vol. 3, no. 1, pp. 5-13, January 1992 (with N. M. Nasrabadi).
[25] "A TMS320C25-Based Implementation of Motion-Compensated Interframe Image Coding System," Proc. First Texas Instruments TMS320 Educators Conference, Houston, Texas, pp. 215-228, July 31 –August 2, 1991 (with N. M. Nasrabadi).
[26] "A Self-Organizing Adaptive Vector Quantization Technique," *Journal of Visual Communication and Image Representation*, vol. 2, no. 2, pp. 129-137, June 1991 (with N. M. Nasrabadi and Y. Feng).
[27] "A Multiprocessor System for Interframe Hierarchical Address-Vector Quantization," Proc. 1991 IEEE International Symposium on Circuits and Systems, Singapore, pp. 61-64, June 11-14, 1991 (with F. J. Desjarlais and N. M. Nasrabadi).
[28] "Hierarchical Block Truncation Coding of Digital HDTV Images," *IEEE Transactions on Consumer Electronics*, vol.36, no.3, pp.254-261, August 1990 (with N.M. Nasrabadi, et al.).
[29] "Design and Analysis of Two-Channel High Definition Television Systems," *IEEE Trans. on Broadcasting*, vol. 36, no. 2, pp.175-183, June 1990 (with N.M. Nasrabadi).